Nano Scale Disruptive Silicon-Plasmonic Platform for Chip-to-Chip Interconnection

Definition of plasmonic devices and properties for chip-to-chip interconnection

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Deliverable Responsible

Organization: Athens Information Technology
Contact Person: Emmanouil-P. Fitrakis
Address: Athens Information Technology
19.5 Km Markopoulo Avenue
19002 Peania, Attiki
Greece
Phone: +30 210 668 2721
Fax: +30 210 668 2703
E-mail: mfitrakis@ait.gr

Executive Summary

This document presents the main targeted characteristics for the devices that will constitute the interconnect system we aim to develop. Comments on changes of schedule and new implementation methods are included, where applicable. In all cases of change of schedule, the new dates are earlier than the dates in the proposal Description of Work. Benchmarking data conclude the document.

Change Records

Version	Date	Changes	Author
0.1 (draft)	2012-03-01	Start	Emmanouil-P. Fitrakis (AIT) Ioannis Tomkos (AIT)
0.2 (draft)	2012-05-23	Contributions by all device leaders	Emmanouil-P. Fitrakis (AIT) Ioannis Tomkos (AIT) Victor Calzadilla (TU/e) Martin Sommer (KIT) Argishti Melikyan (KIT) Juan Martinez-Pastor (UVEG) Dries Van Thourhout (IMEC) Alberto Scandurra (ST)
99 (submit)	2012-5-30	benchmarking	Emmanouil-P. Fitrakis (AIT) Christoforos Kachris (AIT) Ioannis Tomkos (AIT) Alberto Scandurra (ST) Victor Calzadilla (TU/e) Martin Sommer (KIT) Argishti Melikyan (KIT) Juan Martinez-Pastor (UVEG) Dries Van Thourhout (IMEC)

Contents

1. Introduction

The plasmonic interconnect system will consist of the following devices:

Table I:

Type	Device	Leader
Transmitter	Plasmonic Nano-Laser	TU/e
Trasnmitter	Plasmonic Modulator	KIT
Receiver	Plasmonic Amplifier	UVEG
Receiver	Plasmonic Photodetector	UVEG
Supporting Components	Waveguide Coupler	KIT
Supporting Components	Noise Filter	IMEC
Supporting Components	Beam Steering	IMEC
Supporting Components	Signal Generation Module	ST

The following sections present the targeted specifications for each of the above devices.

2. Transmitter

The transmitter will consist of the plasmonic nano-laser and the plasmonic modulator.

a) Plasmonic Nano-Laser

We aim to design a plasmonic laser operating at a wavelength around 1.55 μm; however, it is highly possible to end up with a laser operating between 1.4 and 1.5μm. This is because of the bandgap widening, which happens due to the high carrier injection needed to produce enough gain to overcome the large modal loss.

The expected specifications, at cryogenic temperatures, are:

Table II: Parameters for plasmonic laser

Parameter	Expected value
Wavelength	1.4 – 1.55 μm
Driving Voltage	> 1.5 V
Current	> 1 mA (above 3mA at room temperature)

Device Length	> 10 µm
Output Power	100 ± 90 µW

b) Plasmonic Modulator

Based on the initial experiments, the plasmonic phase modulator is expected to have an internal impedance >> 50 W.

Target specifications can be found below:

Table III: Parameters for plasmonic modulator

Parameter	**Targeted Value**
Overall loss	< 30 dB
Length	< 50 µm
Latency	> 10 µm
Driving Voltage	≤ 4.5V_{pp}

For more information on the plasmonic modulator, see Milestone 9.

3. Receiver

The receiver will consist of the plasmonic pre-amplifier and the plasmonic photodetector.

a) Plasmonic Amplifier

The amplifier will be based on quantum dot gain for surface plasmon-polariton (SPP) propagation on quasi-1D or 2D metal waveguides.

Table IV: Parameters for plasmonic amplifier.

Parameter	**Targeted Value**

On-chip gain	10 dB
Gain with electrical injection	10 dB/cm

b) Plasmonic Photodetector

The goal here is a small footprint and highly sensitive solution for small light signal or direct SPP detection, depending on chip configurations.

Table V: Parameters for plasmonic photodetector.

Parameter	**Targeted Value**
Quantum Efficiencies	> 80%
Responsivities	> 0.1 A/W

4. Supporting components

The supporting components include the waveguide couplers, beam steering, the noise filters and the signal generation module.

a) Waveguide Couplers

An example of the geometrical parameters of the 50 nm slot width plasmonic coupler can be found in the following table.

Table VI: Parameters for waveguide coupler.

Parameter	**Value**
SOI device layer thickness	220 nm
Silicon waveguide width	500 nm
Plasmonic slot width	50 nm
Distance *d*	75 nm

Angle θ	36°
Efficiency of a single coupler	87%

For more information on the waveguide coupler, see Milestone 25.

b) Beam Steering

Table VII: Parameters for beam steering.

Parameter	**Targeted Value**
Distance	1 mm
Bandwidth	> 10 nm
Efficiency	> - 3 dB

It is not yet clear if these specs are actually achievable. This will require further design effort. We also have to define if these are really useful specs. As an alternative approach we are currently investigating MEMS-like steerable gratings.

Implementation:

- classical gratings with shallow etch grooves in silicon,
- metal gratings,
- MEMS-movable grating.

Planning (proposal):

M12 – Design ready

M18 – Fabrication ready

M21 - Fully characterized devices

M24 – Design second generation

M30 – Fabrication second generation

M33 – Second generation fabricated

Planning (actual):

- Design (gen I) implemented on epixfab run August (M10)
- Fabrication completed December (M14)

c) Noise Filter

Table VIII: Parameters for noise filter.

Parameter	**Targeted Value**
Bandwidth	3 nm
Suppression	10 dB
Free Spectral Range	30 nm

Proposed implementation: AWG with flat-top passband (MMI-input based).

Planning (proposal):

M12 – Design ready

M18 – Fabrication ready

M21 - Fully characterized devices

Planning (actual):

- Design implemented on epixfab run August (M10)
- Fabrication completed December (M14)

d) Signal Generating Module (DDCM)

The Dual Die Communication Module (abbreviated DDCM) is the building-block responsible for the interconnection of different dice within a so called Network in Package (NiP), the communication system enabling inter dice data transmission in the context of Systems in Package (SiP) technology.
According to a widely used approach, the DDCM is considered composed of two main building blocks:

- the DDCM controller, responsible for managing incoming/outgoing STNoC traffic and IDN segments, generating them through STNoC flits encapsulation and preparing them to be sent to the PHY transmitter, as well as collecting them from the PHY receiver;
- the DDCM PHY, responsible for transmitting output phyts across the physical link and collecting inputs phyts from the physical link.

The DDCM is a parametric design, configurable in terms of hardware structure specifying the proper set of parameters depending on the context where it has to be used. Moreover the DDCM is programmable via a set of software-programmable registers, allowing to modify its behaviour in real-time, so as to react to changing boundary conditions.
The next figure shows the DDCM structure in terms of top level building-blocks.

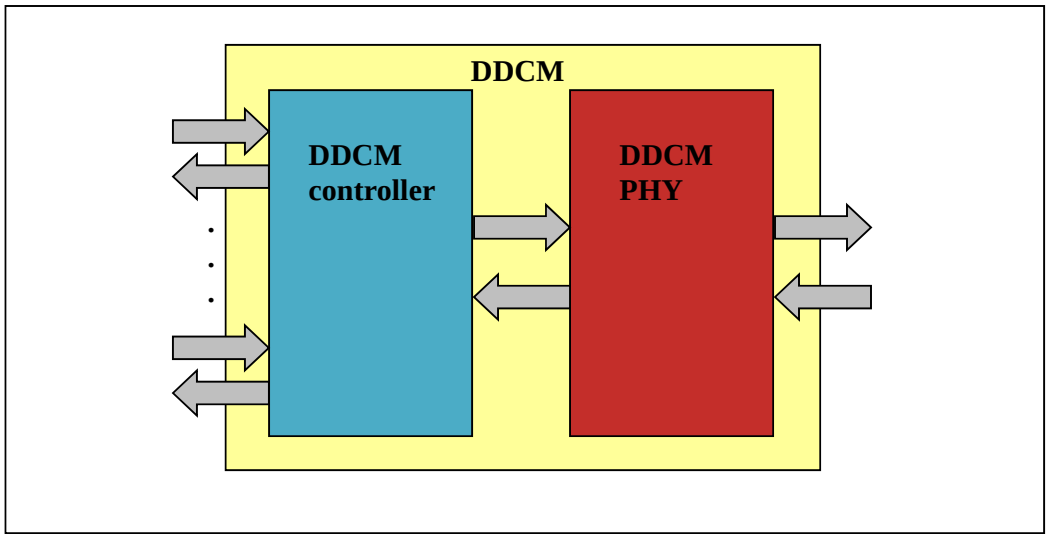

Figure 1: DDCM top level structure

Figure 2 shows the architecture of the DDCM highlighting the connections with initiators and targets across an STNoC interconnect.
Figure 3 shows instead the connection and the traffic streams flows between two dice, highlighting the two DDCMs architectures and their crossing. Specifically, the orange line represents the request traffic stream flowing from initiator 1 in die #1 towards target

2 in die #2, while the yellow line represents the response traffic stream flowing from target 2 in die #2 towards initiator 1 in die #1.

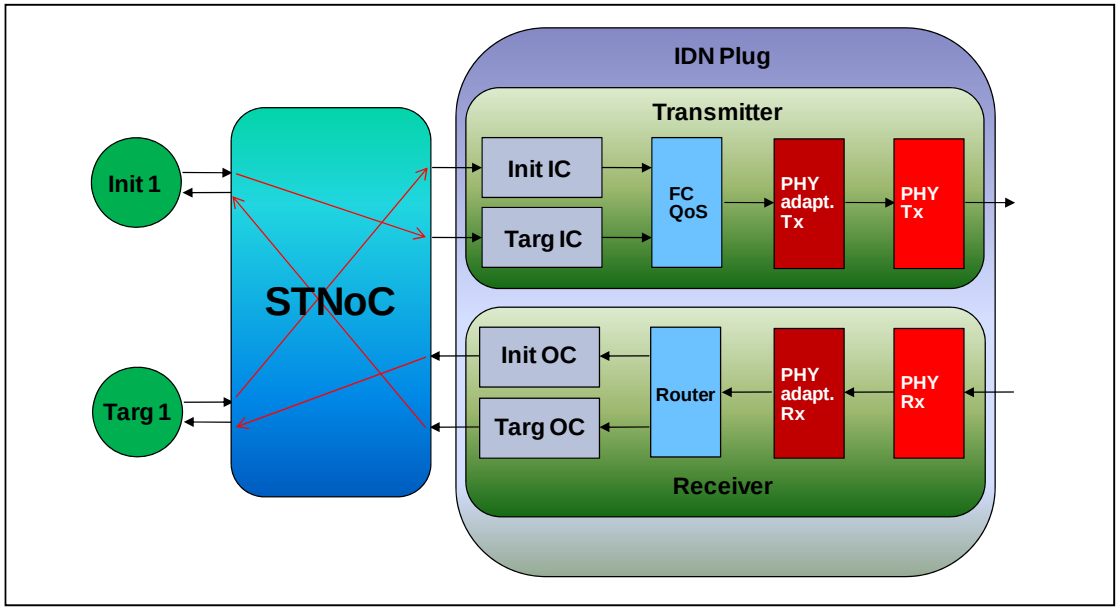

Figure 2: DDCM architecture

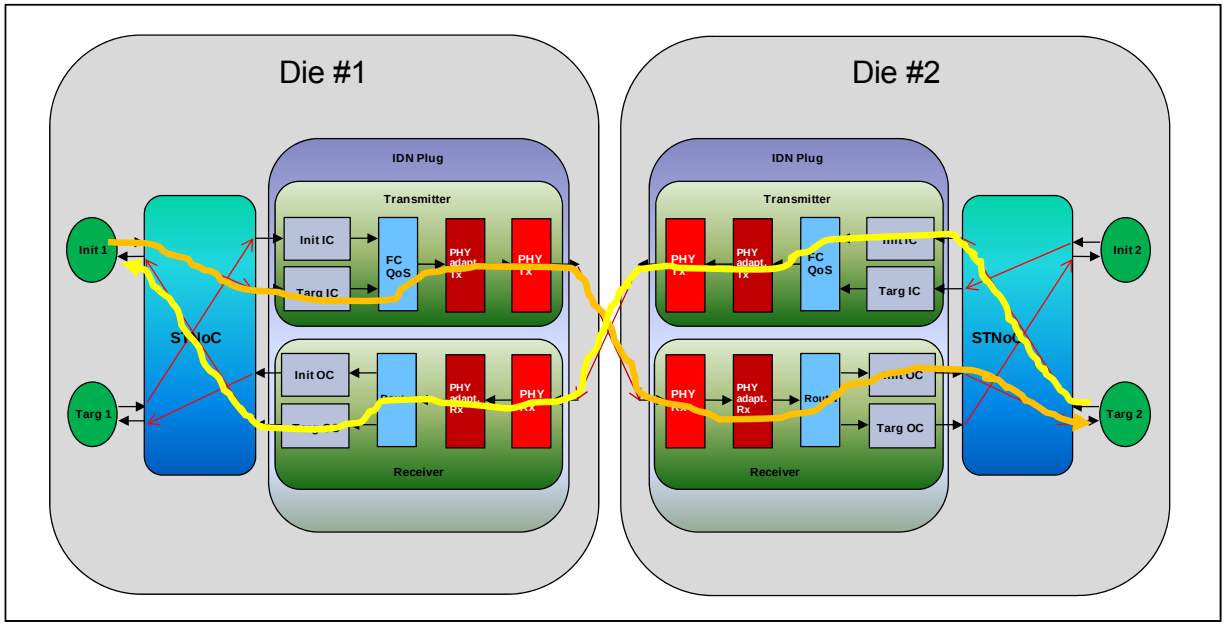

Figure 3 : Traffic streams flows between two dice

For any details about DDCM architecture and microarchitecture please refer to D5.1.

The DDCM will be designed exploiting the CMOS technology available at the time of the implementation phase. Current prototypes are being designed exploiting 40nm, 32nm and 28nm CMOS technologies.
Final DDCM implementation will be likely based on 22nm CMOS technology.

5. Benchmarking & Targets

The desired **data rate** capability for all devices is **7.2 Gb/s**. The desired net **latency** for the plasmonic system is **< 8.88 ns** at 450 MHz clock frequency. In case of faster electronics, latency will have to be lower in order to be competitive.

In 2010, the state-of-the-art optical transceivers consumed tens of pJ/bit [1].

Benchmarking data follows:

Table IX: Benchmarking

Link	Type	Throughput	Latency	Power	Pins
Intel 50G Link [2]	Opt.	50 Gb/s (12.5x4)			
UNIC [1]	Opt.	5 Gb/s*		5 mW*	
TI C2C [3]	Electr.	6.4 Gb/s	50 ns		16
MIPI LLI [4]	Electr.	5.8 Gb/s	80 ns	15pJ/bit	4
MIPI UniPort [4]	Electr.	3.2 Gb/s (0.8x4)	high	15pJ/bit	4

*first-year results of research project.

Intel's 50G Silicon Photonics Optical Link uses lasers to transmit data between two silicon chips, a transmitter and a receiver. It is composed of four optical channels, each running at 12.5 Gb/s, which are combined onto a single fiber to transmit data up to 50 Gb/s.

The Ultra-performance Nanophotonic Intrachip Communication (UNIC) is a DARPA-funded project that involves Sun/Oracle, Kotura and Luxtera. It started in 2008 and finishes in 2013. UNIC aims to achieve “unprecedented high-density, low-power, large-bandwidth, and low-latency optical interconnect for highly compact supercomputer systems”. UNIC first-year achievements included a 320 fJ/bit hybrid-bonded optical transmitter and a 690 fJ/bit hybrid-bonded optical receiver. The project utilizes silicon photonics and assumes an external laser. In 2010, the power consumption target for 2012 was 300 fJ/bit, two orders of magnitude lower than state-of-the-art optical transceivers.

TI C2C (available since 2010) contains technology from Texas Instruments and Arteris. It was created to allow DRAM memory sharing for reduced eBoM cost through a very low latency interface. C2C does not require a PHY. C2C requires about 30 pins total in a mobile phone use model (16 transmit pins, 8 receive pins, plus clock and power pins). Round trip latency is 100 ns. It requires 1.2 or 1.8 volts and has throughput of 6.4 Gb/sec at 200 MHz DDR speeds and using 16 pins.

The UniPro specification was first released in 2007. UniPort is UniPro combined with a MIPI D-PHY or M-PHY. It supports a maximum data rate of 800 Mbit/s per lane, for 1 to 4 lanes. UniPro is not low latency enough for RAM sharing.

The MIPI LLI specification was released in 2011, but we only have targeted specs. Its primary purpose was to allow sufficient performance to enable sharing a DRAM memory. The main motivation was electronic bill of materials (eBoM) cost reduction. Round trip latency was targeted to be 80 ns using 8 pins in Gear 3. Unidirectional throughput is 2.9 Gb/s per lane using Gear 2.

[1] G. L. Li, X. Z. Zheng, J. Lexau, Y. Luo, H. Thacker, T. Pinguet, P. Dong, D. Z. Feng, S. R. Liao, R. Shafiiha, M. Asghari, J. Yao, J. Shi, I. N. Shubin, D. Patil, F. Liu, K. Raj, R. Ho, J. E. Cunningham, and A. V. Krishnamoorthy, “Ultralow-power silicon photonic interconnect for high-performance computing systems,” Optoelectronic Interconnects and Component Integration IX7607, 760703 (2010).
[2] The 50G Silicon Photonics Link, Intel White paper, July 2010

[3] Texas Instruments Chip-to-Chip Link (C2C),

http://www.arteris.com/c2c_chip-to-chip_for_DRAM_memory_sharing

[4] MIPI Alliance, http://www.mipi.org/

[5] http://synopsys.mediaroom.com/index.php?s=43&item=836